ABSTRACT

Disclosed is a method of fabricating a multi-layered PCB, wherein a plurality of circuit layers on which circuit patterns are constructed and insulating layers which are alternately positioned between the circuit layers to insulate the circuit layers from each other are severally fabricated according to different processes, and then layered with each other at once.

The present invention provides a method of fabricating a multi-layered PCB, in which a copper clad laminate is drilled to create via holes therethrough in such a way that a diameter of each via hole is relatively small, and then plated with copper to plug the via holes with the copper, thereby omitting the plugging process of the via holes using paste. The insulating layers are formed in such a way that semi-hardened (b-stage) thermosetting resin layers are layered on both sides of a completely hardened (C-stage) thermosetting resin layer, thereby improving impedance balance of the insulating layer.